SIGNAL NAME	PLACE OF ORIGIN (BOARD OR OTHER SOURCE)	SIGNAL TYPE	DIGITAL FORMAT	DESCRIPTION
1 CM/MIN	S102	SW	L	Control bit from the rear-panel CHART SPEED switch sent to the recorder CPU.
1.1 KHZ	5802 or 6802	D	H<—>L	Used as a time base (RST 7.5) by the supervisor CPU, the ECG AGC circuit "sample-and-hold" counter (5807 Board), and the chassis-mounted ECG beep circuits.
±1.2 V HR	5802	A		Processed analog heart-rate voltage (single-cardiotach) sent to rear-panel systems connector (J102). –1.2 V = 0 bpm +1.2 V = 240 bpm
±1.2 V HR1	6802	A		Processed analog heart-rate voltage (dual-cardiotach) sent to rear-panel systems connector (J102). –1.2 V = 0 bpm +1.2 V = 240 bpm
±1.2 V HR2	6802	A		Second processed analog heart-rate voltage (dual-cardiotach) sent to rear-panel systems connector (J102). –1.2 V = 0 bpm +1.2 V = 240 bpm
±1.2 V PRESS	5802 or 6802	A		Processed analog voltage representing pressure signal routed to the rear-panel systems connector (J102). –1.2 V = 0 mmHg +1.2 V = 100 mmHg
2 (4)	5802 or 6802	D	H	Bus for BCD word representing numerics data for front-panel heart-rate display.
+4 V	5800	R		Reference voltage for strain gauge or tocotransducer bridge. Also, DIRECT UA is initiated by current drawn from this reference.
6.144 MHZ	5802 or 6802	D	H<—>L	CPU clock used by the supervisor and recorder microprocessors.
8 HZ	5802 or 6802	D	H<—>L	ECG time-base clock (5807 Board).
9 KHZ	5802 or 6802	D	H<—>L	Clock for rate-discriminator counter (5807 Board); timer in for I/O port (Recorder Board).
+10 V	5800	R		Reference used for heart rate and pressure DACs located on CPU Board.

SIGNAL NAME	PLACE OF ORIGIN (BOARD OR OTHER SOURCE)	SIGNAL TYPE	DIGITAL FORMAT	DESCRIPTION
–V CONV	5800			Not used.
36 KHZ	5800	D	H<—>L	Clock signal used by isolated and non-isolated ECG circuits. (Divided 36 kHz derivatives used for CPU and ECG time bases.) **IMPORTANT!** This signal must always be available on the 5806 Board. Otherwise, the 5806 Board may be damaged.
80 HZ PHONO	5800	A		Filtered heart-sound audio signal used on the Correlator Board.
AGC'd PHONO	5806	A		Automatic-gain controlled heart-sound signal used by phono processing circuits on 5800 and 5806 Boards.
AUDIO	5800	A		Low-level audio from switches.
AUDIO OUT	5800	A		Audio power output to rear-panel speaker.
BLANK	5802 or 6802	D	L	Not used.
CR	5808, 6709, 6808, 6665, or 6666	D	L	Clears printhead shift registers; goes low on power-up OR if a head shutdown occurs.
DAC OUT	5802 or 6802	A		Audio signal level-controlled by front-panel VOL pushbuttons via supervisor CPU.
DIRECT UA	5800	D	H	Enable generated by current drain on the +4-V reference (5800 Board). This enable is generated by a strain gauge but not by a tocotransducer. However, the supervisor CPU ignores DIRECT UA if TOCO (pin F, CPU Board) is high.
DOT CLK	5808, 6709, 6808, 6665, or 6666	D	H<—>L	Clock signal DOT DATA going into the printhead serial-in/parallel-out shift registers.
DOT DATA	5808, 6709, 6808, 6665, or 6666	D	<DOT CLK>:<H XOR L>	Bit train written in serially to the printhead shift registers representing a column of dot-matrix information. H = black L = white or no-print
ECG	J2	SW	L	FECG or MECG control bit generated by jumper in leg-plate plug or maternal cable, respectively, sent to the supervisor CPU to identify ECG mode. (See FECG and MECG.)

SIGNAL NAME	PLACE OF ORIGIN (BOARD OR OTHER SOURCE)	SIGNAL TYPE	DIGITAL FORMAT	DESCRIPTION
ECG +80 dB	5806	A		Same signal as ECG amplified by 1000 but with an additional 20 dB of gain. This signal is routed to the rear-panel jack.
ECG BEEP	5802 or 6802	D	H	FET-switch enable (5800 Board) which applies 1.1-kHz to audio preamp for every ECG event pulse.
ECG EVENT	5807	D	H<—>L	FECG or MECG pulse train from the 5807 board sent to the supervisor CPU for FHR or MHR computations.
ECG NOTCHED	5806	A		Same signal as ECG +80 dB but with any residual line-frequency noise removed with a high-Q notch filter.
ECG TEST (+)	5807	D	H<—>L	2-Hz pulse train sent to rear-panel leg-plate tester. (2 Hz corresponds to a FHR of 120 bpm.)
ECG x 1000	5806	A		FECG or MECG signal sent to the rear-panel systems connector (J102) multiplied by a factor of 1000.
EVENT OUT	5806	D	H<—>L	Pulse train sent to the CPU Board for HR computations.
EXT BAT (+)	P13	PS		Connections from (+) terminal of internal battery used to maintain calendar/clock when monitor AC power is disconnected.
EXT FHR	5802 or 6802	D	L	CMOS compatible low-true signal which indicates that the monitor is in either the phono or ultrasound mode. This signal is routed to the rear-panel systems connector (J102).
FECG	J2	SW	L	Control bit, generated by jumper in leg-plate plug, sent to the supervisor CPU to identify ECG mode.
FETAL INHIBIT	5807	D	L	Low "inhibits" peak-detected 30 Hz fetal signal from affecting error-amplifier capacitor, C5 (5806 Board). High pulse occurs with a heartbeat event pulse and transfers peak-detected 30-Hz voltage from C1 to C5 (5806 Board).
FETAL CAP RESET	5807	D	H	Signal used to reset the sample-and-hold capacitor (C1) in the ECG AGC loop.

SIGNAL NAME	PLACE OF ORIGIN (BOARD OR OTHER SOURCE)	SIGNAL TYPE	DIGITAL FORMAT	DESCRIPTION
HD SHUTDOWN	5808, 6709, 6808, 6665, or 6666	D	H	Result of PAPER OUT or STB <1-4> in excess of 7 ms. Causes power supply to shut down power to printhead (see V HD).
HEADSET JACK	J104	A		This signal is DAC OUT which is first routed to the rear-panel headset jack (J104). If no headset is inserted in the jack, the signal is routed to the 5800 Board to the audio power amplifier for the internal speaker.
HEARTBEAT LED	5802 or 6802	D	L	Enable for front-panel heartbeat indicator display (5812 Board).
HR INOP	5802 or 6802	D	H	CMOS-compatible signal routed to the rear-panel systems connector (J102). A high indicates no HR transducers are plugged into the front-panel connectors.
LA	J2	A		Connection from "red" post of leg plate, or "black" terminal from maternal cable, routed to the 5806 Board.
LOAD	5808, 6709, 6808, 6665, or 6666	D	L	Strobe which transfers dot data from serial-in/ parallel-out shift registers in printhead to heater-element latches and associated gates. Dot data is transferred to element transistors when STB lines go low.
MARK	5812	SW	L	Front-panel switch for the Mark pushbutton.
MECG	J2	SW	L	Control bit, generated by jumper in maternal cable, sent to the supervisor CPU to identify ECG mode.
NEW PEAK	5806	D	L—>H—>L	Comparator output which toggles on a threshold and peak-detector capacitor charge ECG peak which exceeds the threshold value. (Used in 262-bpm inhibit circuit.)
OPTO DRIVE A	5808, 6709, 6808, 6665, or 6666	PS		Positive supply for "Paper-Low" optosensor LED.
OPTO DRIVE B	5808, 6709, 6808, 6665, or 6666	PS		Positive supply for "Paper-Out" optosensor LED.

SIGNAL NAME	PLACE OF ORIGIN (BOARD OR OTHER SOURCE)	SIGNAL TYPE	DIGITAL FORMAT	DESCRIPTION
PAPER ADV	5812	SW	L:L—>H	Low (Paper Advance button depressed) causes the recorder CPU to advance paper at 25 cm/min. The L—>H transition (button released) causes the supervisor CPU to output mode, time, and date after 20 seconds.
PAPER LOW	P25	D	H	Reflection of drive LED from chart paper causes optosensor to conduct holding PAPER LOW low. Black squares near end of chart result in insufficient reflection and PAPER LOW goes high alerting recorder CPU.
PAPER OUT	P24	D	H	Reflection of drive LED from chart paper causes optosensor to conduct holding PAPER OUT low. If paper runs out, reflection from black roller is insufficient and PAPER OUT goes high alerting recorder CPU.
PEAK DETECTOR INHIBIT	5807	D	H	Inhibits peak detector (5806 Board) at the end of a 228-ms blanking period prior to resetting and prior to the output of an ECG event pulse.
PEAK DETECTOR RESET	5807	D	H	Resets rate discriminator peak detector at the end of a 228-ms blanking period.
PENLIFT 2	5802 or 6802	D	H	CMOS-compatible version of PENLIFT OUT which is also routed to the rear-panel systems connector.
PENLIFT IN	S103	D	L	Goes low when the rear-panel ECG ARTIFACT ELIMINATION switch is in the ON position.
PENLIFT OUT	5802 or 6802	D	H	Open-collector output to control the penlift of older-style strip-chart recorders. pen lifted = open pen down = low
PHONO	J1/5800	D	L/H	Low enable generated by jumper in phonotransducer plug. PHONO high is an inverted version gated through by ECG high (5800 Board).
PHONO EVENT	5801 or 7180	D	L<—>H	FECG pulse train sent from the Correlator Board to the supervisor CPU for FHR computations.
PHONO IN	Phonotransducer	A		Low-level audio signal from phonotransducer representing fetal heart sounds.
PHONO POWER	5800	PS		+12-V loaded supply for phono preamplifier located in the phonotransducer body.

SIGNAL NAME	PLACE OF ORIGIN (BOARD OR OTHER SOURCE)	SIGNAL TYPE	DIGITAL FORMAT	DESCRIPTION
PHONO REF	5800	PS		Return for PHONO POWER.
POLARITY CORRECT	5806	D	H	Holds autopolarity control timer (U7, 5807 Board) reset if polarity sense is positive.
POLARITY CONTROL	5807	D	H or L	Level which toggles and reverses R-wave polarity if sense is incorrect.
+PRESS	Tocotransducer or Strain Gauge	A		Incrementing differential output from strain gauge or tocotransducer bridge.
–PRESS	Tocotransducer or Strain Gauge	A		Decrementing differential output from strain gauge or tocotransducer bridge.
PRESS OFF-SCALE LED	5802	D	L	Enable for front-panel "BASELINE PRESSURE OFFSCALE" display.
PRESS ZERO	5812	SW	L	Switch for the UA Reference pushbutton.
Q-4	5808, 6709, 6808, 6665, or 6666	D	L	Open-collector returns for the recorder stepper motor (J18).
RA	J2	A		Connection from "green" post of the leg plate, or "white" terminal from maternal cable, routed to the 5806 Board.
REC b (8)	5802 or 6802	D	H	Unidirectional data bus from supervisor CPU to recorder CPU. A transfer consists of a control word (8 bits) followed by a 0 to 7 word message string.
RECORD	5812	SW	L	Front-panel Record pushbutton switch.
RECORD LED	5802 or 6802	D	H	Enable from supervisor CPU to front-panel LED indicating recorder is activated.
REC OBF	5802 or 6802	D	L	I/O control signal sent to recorder CPU indicating supervisor CPU has data to send (see REC b).
REC TRAP	5802 or 6802	D	H	Restart interrupt initiated by supervisor CPU if recorder CPU fails to respond to REC OBF with SUP ACK within a reasonable period of time.

SIGNAL NAME	PLACE OF ORIGIN (BOARD OR OTHER SOURCE)	SIGNAL TYPE	DIGITAL FORMAT	DESCRIPTION
RESET	5802 or 6802	D	H	A RESET IN to the supervisor CPU during power-up causes a RESET OUT (8085 microprocessor function) which is used to hold system functions, such as the correlator and recorder CPUs, reset until the supervisor CPU completes its reset.
RL	J1	A		Connection from conductive leg-plate face, or "green" terminal from maternal cable, routed to the 5806 Board.
SHIELD	5806	A		Used for AC line-noise suppression or shield surrounding leg-plate leads.
SPEED OVERRIDE	J102	D	L	CMOS-compatible input from rear-panel systems connector which causes the supervisor CPU to begin recording HR and UA data at the highest available trending speed.
STB 1-4	5808, 6709. 6808, 6665 or 6666	D	L	Strobes which enable printhead heater gates (see LOAD).
SUP ACK	5808, 6709, 6808, 6665, or 6666	D	L	I/O control signal sent to supervisor CPU indicating recorder CPU is ready to receive data (see REC b).
SUP PAPER LOW	5808, 6709, 6808, 6665, or 6666	D	L	Recorder-to-supervisor CPU control bit indicating black squares on chart paper have been detected by the "Paper-Low" optosensor.
SUP RDY TO REC	5808, 6709, 6808, 6665, or 6666	D	L:L—>H	Low prevents supervisor CPU from trapping recorder CPU while the latter is in a self-test mode. The L—>H transition signals the supervisor CPU that the recorder CPU has completed its test.
T/D EN	S101	SW	L	Low when the rear-panel TIME/DATE SET switch is in the ENABLE position. Causes supervisor CPU to put monitor in time/date set mode while disabling all other monitor functions.
TD SEL	P6	SW	L	CPU Board time/date parameter select active when T/D EN is low (S101).
TD <up/down arrows>	P6	SW	L	Time/date set increment/decrement enables active when T/D EN is low (S101).
TELEMETRY	J102	D	L	CMOS-compatible input from rear-panel systems connector indicates to the supervisor CPU that telemetry monitoring is in use. (Causes the message "TELEMETRY" to be printed on strip chart at power-on if telemetry, ECG, and TOCO enables are all active).

SIGNAL NAME	PLACE OF ORIGIN (BOARD OR OTHER SOURCE)	SIGNAL TYPE	DIGITAL FORMAT	DESCRIPTION
TEST	5812	SW	L	Front-panel Test pushbutton switch.
TOCO	J3/5800	D	L/H	Low-enable generated by jumper in tocotransducer plug. High TOCO is inverted version generated on the 5800 Board.
TRC	5802 or 6802	D	H	Rear-panel systems connector pin (J102) indicating that a tocotransducer is in use. 0 V = Toco in use –15 V = Toco not in use
UA INOP	5802 or 6802	D	H	CMOS-compatible high signal indicating monitor is in the self-test mode OR that neither a toco nor a strain gauge is plugged into the front-panel UA connector. This signal is routed to the rear-panel systems connector (J102).
UA TEST	5802 or 6802	D	H	Enable which causes 50 mmHg offset in pressure channel (5800 Board) during self-test initiated by front-panel Test pushbutton.
UA V/F	5800	D	H<—>L	Voltage-to-frequency clocked waveform representing –50 to 200 mmHg offset.
U/S	J1(5802 or 6802)	D	L & H	U/S low is an enable produced by a jumper in the ultrasound transducer plug. U/S high is an inverted version gated on by ECG high (CPU Board).
U/S AUDIO	5800	A		Detected and filtered (200-600 Hz) ultrasound audio signal.
U/S EVENT	5801 or 7180	D	L<—>H	FECG pulse train sent from the Correlator Board to the supervisor CPU for FHR computations.
U/S PHONO ENABLE	5806 on-board	D	H/L	This signal is U/S from the 5807 Board. However, although U/S high indicates ultrasound, a U/S low here is interpreted as a phono mode enable regardless of actual monitor mode in use.
U/S RECV	Ultrasound Transducer	A		Doppler-shifted receive signal of fetal echo representing heart motions.
U/S XMIT	5800	A		2.3-MHz cw power for ultrasound transducer.
V HD	5804	PS		Protected power source for the thermal printhead elements; disabled if HD SHUTDOWN goes high.

SIGNAL NAME	PLACE OF ORIGIN (BOARD OR OTHER SOURCE)	SIGNAL TYPE	DIGITAL FORMAT	DESCRIPTION
VOL <up/down arrow>	P6	SW	L	CPU-Board increment/decrement enables for software controlling audio DAC.
XFER1	5802 or 6802	D	L	Strobe used to enable hundred's digit display (5812 Board).
XFER2	5802 or 6802	D	L	Strobe used to enable ten's digit display (5812 Board).
XFER3	5802 or 6802	D	L	Strobe used to enable unit's digit display (5812 Board).
XFER <up arrow>	5802 or 6802	D	H—>L:L—>H	100-ms low-going pulse (routed to rear-panel systems connector, J102) which occurs after each valid event trigger. The rising edge may be used to strobe ±1.2 V HR (HR1 or HR2 if dual-cardiotach) and ±1.2 V UA outputs into a data acquisition system.

ANALOG/DIGITAL SIGNALS SUMMARY
TABLE 4-22